IEEE Quantum Week Workshop:
Ultra-low Power Electronics for Superconducting Quantum Processors

Agenda

Session 1: 10:45-12:15 (MDT) — UTC-6

	10:45-10:51	6 min	**Frank Wilhelm-Mauch**	Opening
1	10:51-11:29	35 + 3 min	**David J. Frank**	• Introduction to quantum computing control systems • Hardware control considerations for a large-scale transmon quantum computer
2	11:29-11:52	25 + 3 min	**Christian K. Andersen**	Design of superconducting quantum devices for quantum error correction with the surface code

Session 2: 13:00-14:30 (MDT) — UTC-6

3	13:00-13:30	25 + 5 min	**Steven Brebels**	CMOS cryo-electronics for superconducting quantum processors
4	13:30-14:00	25 + 5 min	**Anna, Quentin Herr**	Superconducting digital technology for quantum computing
5	14:00-14:30	25 + 5 min	**William D. Oliver**	Quantum Engineering of Superconducting Qubits

Session 3: 15:15-16:45 (MDT) — UTC-6

6	15:15-15:48	30 + 3 min	**Rüdiger Quay & Carsten Degenhardt**	Systems engineering for scalable quantum computing
	15:48-16:38	40 + 10 min	**David J. Frank** **Christian K. Andersen** **William D. Oliver** **Anna Herr** **Steven Brebels** **Rüdiger Quay & Carsten Degenhardt** **John Martinis**	Panel discussion Chair: **Frank Wilhelm-Mauch**
	16:38-16:45	7 min	**Anton Potocnik**	Closing remarks

Abstracts

1. Hardware control considerations for a large-scale transmon quantum computer

David J. Frank
IBM Watson Research Center, PO Box 218, Yorktown Heights, NY 10598

We will discuss architectural considerations for large-scale quantum computing based on transmons and some of the likely control hardware requirements for such a computer. Quantum computing offers the possibility of solving some types of problems much faster than classical computation. To achieve this speed up, it is expected that such a computer may need 1 million or more physical qubits, organized into logical qubits whose quantum states are stabilized using quantum error correction. Based on these ideas, we can make some estimates of requirements that will be necessary to make this work, such as qubit coherence, gate fidelity, activity factor, power, speed, and size. This will lead to consideration of how cryogenic electronics may be able to facilitate such a system. Finally, we will discuss some of IBM's plans to build a 1000 qubit system as a step along the way to building a large-scale quantum computer.

2. Design of superconducting quantum devices for quantum error correction with the surface code

Christian K. Andersen
TU Delft, Netherlands

Quantum error correction is a key challenge in the field of quantum computing and a next milestone to be passed is to demonstrate the correction of bit- and phase-flip errors on a logical qubit. A promising approach to quantum error correction is the surface code, where physical qubits are arranged into a 2D grid. In this talk, I discuss how the surface code can be implemented with superconducting qubits. I will present the design of a device with 7 superconducting qubits, which was designed to implement an instance of the surface code. I will demonstrate how this device was used to run repeated quantum error detection which yielded logical quantum states with a lifetime and a coherence time longer than those of any of the constituent qubits when no errors are detected. I will finally present an outlook and challenges for performing quantum error correction with superconducting qubits.

3. CMOS cryo-electronics for superconducting quantum processors

Steven Brebels
imec
Leuven, Belgium

The interconnection between the qubits operating at cryogenic temperatures and room temperature classical electronics for qubit control and readout becomes increasingly challenging when increasing the number of qubits in the quantum computer. Since nano-scale CMOS transistors function well below 10 K, CMOS circuitry can de designed as interface between qubits and interconnect wires. In this talk we will discuss two examples of interface circuits: a microwave multiplexer operating near base temperature and a 4 K dispersive readout circuit. These circuits demonstrate the challenges for analog CMOS circuit design at cryo-temperatures including device modelling and ultra-low power operation.

4. Superconducting digital technology for quantum computing

Anna Herr, Quentin Herr
imec
Leuven, Belgium

Superconducting digital technology has long been advocated as a suitable classical interface for superconducting qubits. Compatibility in energy levels, operating temperature, materials and fabrication processes are common arguments in favor of a fully superconducting solution for an integrated classical-quantum processor. In such a system classical superconducting circuits have advantages in record low power dissipation and speed with the potential to provide unique performance at all levels of the computing stack from decoding and data preparation, to the mixed-signal interface with the qubits. In practice, application of superconducting digital circuits for quantum computing has been limited to a few pioneering experiments. Maturation of superconducting digital technology has not reached a level to be widely accepted by the quantum community. In this workshop we will review status of superconducting digital technology and outline the research and development needed to overcome maturation challenges.

5. Quantum Engineering of Superconducting Qubits

William D. Oliver
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Research Laboratory of Electronics, and MIT Lincoln Laboratory
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Quantum computers are fundamentally different than conventional computers. They promise to address problems that are practically prohibitive and even impossible to solve using today's supercomputers. The challenge is building one that is large enough to be useful. In this talk, I will discuss aspects of engineering high-performance superconducting qubits, with an eye

toward extensible applications. After a brief introduction to superconducting qubits [1], I will discuss our approach to 3D integration of high-fidelity devices [2] and the impact of ionizing radiation on qubit performance [3].

1. P. Krantz, *et al.* Appl. Phys. Reviews 6, 021318 (2019) | arXiv:1904.06560
2. D.W. Yost, *et al.,* npj Quantum Information 6, 58 (2020) | arXiv:1912.10942
3. A.P. Vepsalainen, *et al.*, Nature 584, 551-556 (2020) | arXiv:2001.09190

6. Systems engineering for scalable quantum computing

Carsten Degenhardt
Head of Electronic Systems for Quantum Computing

Forschungszentrum Jülich GmbH
Central Institute of Engineering, Electronics and Analytics
ZEA-2 – Electronic Systems

We will give an overview of our activities on systems engineering for truly scalable quantum computing by using cryogenic electronics. The top-down system considerations including co-simulations of electronics and qubits allow for optimized partitioning of the electronics. In a bottom-up implementation we design, implement and test building blocks for qubit control and readout in state of the art CMOS processes at 65nm and 22nm in combination with ultra-low noise cryogenic metamorphic HEMT. These span components like bias DACs, voltage references and regulators and microwave mixers. Further, the integrated scaling of arrays of mHEMT receivers is discussed.